Nation of Allowability	Application No.	Applicant(s)
	10/813,267	IOVIN ET AL.
Notice of Allowability	Examiner	Art Unit
(Bryce P. Bonzo	2113
The MAILING DATE of this communication appea All claims being allowable, PROSECUTION ON THE MERITS IS (On herewith (or previously mailed), a Notice of Allowance (PTOL-85) on NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGOR of the Office or upon petition by the applicant. See 37 CFR 1.313	OR REMAINS) CLOSED in this appropriate communication ithe appropriate communication ithe application is subject to	plication. If not included will be mailed in due course. THIS
1. \boxtimes This communication is responsive to <u>the Application as filed</u> .		
2. ⊠ The allowed claim(s) is/are <u>1-24</u> .		
3. Acknowledgment is made of a claim for foreign priority und a) All b) Some* c) None of the: 1. Certified copies of the priority documents have be completed to the priority document has the priority document have be completed below. Failure to timely comply will result in ABANDONME this three-Month period is not extrembable. 4. Applicant has the priority document has a submitted be priority documents have be completed by the Notice of Draftsperson of the priority documents have be completed by the Notice of Draftsperson of the priority documents have be submitted by the Notice of Draftsperson of the priority documents have be completed by the Notice of Draftsperson of the priority documents have be completed by the Notice of Draftsperson of the priority documents have be completed by the Notice of Draftsperson of the priority documents have be completed by the Notice of Draftsperson of the priority documents have be completed by the Notice of Draftsperson of the priority documents have be completed by the Notice of Draftsperson of the Priority documents have be completed by the Notice of Draftsperson of the Priority documents have be completed by the Notice of Draftsperson of the Priority documents have be completed by the Notice of Draftsperson of the Priority documents have be completed by the Notice of Draftsperson of the Priority documents have be completed by the Notice of Draftsperson of the Priority documents have be completed by the Notice of Draftsperson of the Priority documents have be completed by the Notice of Draftsperson of the Pr	peen received. peen received in Application No peen received in Application No pen received in Application No pen received in Application No pen received in this application. The submitted in the Section of the Comment of the Comme	national stage application from the complying with the requirements 'S AMENDMENT or NOTICE OF tion is deficient. 948) attached office action of the back) of the complying with the front (not the back) of the complying in the submitted. Note the
Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. Notice of Informal Pa 6. Interview Summary Paper No./Mail Date 7. Examiner's Amendm 8. Examiner's Stateme 9. Other	(PTO-413), e

Reasons for Allowance

Claims 1-24 are allowed. Below is the reasoning for this indication of allowable subject matter. Applicant is reminded the claims are allowed as a whole, and any modification to the claims may result in a removal of allowability.

Claims 1-6 contain the following features in combination:

- 1. A debugging system comprising:
- a host system to observe and control the step-by-step execution of a debugging operation;
- a target system communicatively coupled to the host system, the target system including
 - a debug port having a plurality of pins;
 - a debug port interface coupled to the debug port; and
- a power management pin separate from said plurality of pins and not coupled to the debug port via the debug port interface; and
- a connection to couple one of said plurality of pins to said power management pin, said connection being independent of said debug port interface.

The cited prior art does not describe the particular arrangement of pins of a debug port and connections to the power management pin as shown above.

Claims 7-9 and 16-18 contain the following features in combination:

7. A method of debugging, comprising:

sampling a power management signal on a device, the power management signal being separate from a test access port of the device;

determining whether a power management transition has occurred on the based on the power management signal; and

triggering a debug mode if a power management transition has occurred.

The cited prior art does not describe the use of management signals. The prior art's closest comparable technology checks error status signals at power up, but does not initiate debugging on the management signals accord.

Claims 10-12 and 19-21 contain the following features in combination:

10. A method of debugging, comprising:

issuing a command to halt execution on a device;

querying a sleep pin on the device to determine whether the sleep pin is asserted;

asserting a system error pin on the device to wake up the device;

querying a stopclock pin on the device to determine whether the sleep pin is de-asserted; and

processing the halt command.

The prior art does not make use of these three pins in this precise manner in debugging.

Claims 13-15 contain the following features in combination:

13. A method of debugging, comprising:

deferring power management transitions on a device;

issuing a test access port scan to the device; and

determining whether a power management transition occurred during the test

access port scan.

The Examiner was unable to find any explicit teaching of how to handle power management transitions in the use of TAP scans. All literature on the subject ignores the power during a TAP scan.

22. A machine accessible medium containing program instructions that, when executed by a processor, cause the processor to:

receive a command that indicates to the processor how to defer power state transitions in a target device;

clear a first bit and a second bit in a designated register of a target device if the command indicates that power state transitions are not deferred; Art Unit: 2113

set the first bit and clear the second bit if the command indicates that power state transitions are always deferred;

set the first bit and clear the second bit if the target device is in debug mode and the command indicates that power state transitions are deferred while the target device is in debug mode; and

clear the first bit and set the second bit if the target device is not in debug mode and the command indicates that power state transitions are deferred after a breakpoint.

As described above, the process of deferring debugging based on a power states was not found, these claims describe the specific memory mechanisms which provide for that deferring.